Binary-encoded Address for All-optical Packet Switching


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Abstract: We experimentally demonstrated the feasibility of binary-encoded packet address header in all-optical packet switching using Fabry-Perot laser diodes. The address length of a network with N output ports is reduced from N to log₂N bits.

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1. Introduction

All-optical packet switching (OPS) is one of the key technologies for future optical networks because it eliminates optical-electrical conversion. Both OPS and hybrid packet switching schemes have been proposed and demonstrated [1,2]. Recently, we have shown that a packet-long control signal can be generated by interaction in a single bit interval at the packet header using a Fabry-Perot laser diode (FP-LD) [3]. We have also demonstrated all-optical packet switching with all-optical header processing with header rate at 10 Gb/s and payload rate of 160 Gb/s [4]. In order to simplify the demand on optical signal processing, we have adopted the self-routing address format [5] where every output port of all the nodes in a network is identified by a single bit in the address. The address length is thus equal to the number of output ports of all the nodes in a network. This scaling of the address length limits the application of the proposed OPS scheme to medium and small size networks. In this paper, we demonstrated an all-optical 1×4 packet switch architecture in which the traditional binary-encoded address format can be used. The proposed architecture can be generalized to 1×N packet switches. Hence, the length of the address can be reduced from N to log₂N bits where N is the total number of output ports of all the nodes in the network. The number of FP-LDs required is also reduced to log₂N.

2. Operating principle

Figure 1 shows the schematic of the architecture of the proposed all-optical 1×4 packet switch for packets with binary-encoded addresses. Each output port is identified by two bits in the packet address header for the four output ports. The addresses for Output 1 to Output 4 are 00, 01, 10 and 11 respectively. The 1×4 packet switch is composed of 2 control packet generators (GENs), 2 signal inverters (INVs) and 4 all-optical switches (AOSs) as shown in the dotted box. When a data packet at wavelength λ_d arrives, copies of the data packet are sent to the GENs. GEN-1 and GEN-2 correspond to the most significant bit and the least significant bit of the header respectively. Different local control signals are sent to the GENs. Each of these two control signals is designed to process one bit in the data packet address. Depending on the value (0 or 1) of the corresponding address bit, the GENs will generate a low level or high level control packet at wavelength λ_c. The function of the INVs is to invert the level of the control packet. Four copies of the data packets are sent into the AOSs. Beside the data packets, AOS-1 receives the control packets from the GEN-1 and GEN-2 while AOS-2 receives the control packets from GEN-1 and the inverted control packets of GEN-2 from INV-2. AOS-3 receives the control packets from GEN-2 and inverted control packets of GEN-1 from INV-1 while AOS-4 receives the inverted control packets of GEN-1 and GEN-2 from INV-1 and INV-2 respectively as shown in Fig. 1. With this arrangement, both of the control packets will be at low level when entering AOS-1, AOS-2, AOS-3 or AOS-4 if the address is 00, 01, 10, or 11 respectively. In all other combinations of addresses and AOSs, one or both of the control packets entering the corresponding AOS will be at high level. We use the multi-wavelength cross-gain modulation property of semiconductor optical amplifiers (SOAs) to implement the AOSs. The AOS will transmit a data packet if and only if both of the control signals are at low level. If one or both of the control packets are at high level, then the AOS will block the transmission of the data packet. As a result, the data packet will exit through Output 1, 2, 3 or 4 if the address is 00, 01, 10, or 11 respectively.

3. Experimental results

Figure 2 shows the experimental setup. The data packets at 1546.150 nm are generated by externally modulating a tunable laser (TL_1) using a 10 Gb/s non-return-to-zero (NRZ) pulse pattern generator (PPG_1) and a 10 Gb/s LiNbO_3 modulator. Four types of packets are used with header addresses 00, 01, 10 and 11 for pk-1, pk-2, pk-3 and pk-4 respectively. The data rates of the packet header and data payload are 5 Gb/s and 10 Gb/s respectively. The packet length is 128 bits and the guard period is 28 bits long. We used a single FP-LD to implement the function of each GEN. For GEN-1, we inject a local signal at wavelength 1551.576 nm (λ_c1) and the input data packets into the FP-LD. The local signal is generated by using a 10 Gb/s NRZ PPG, a 660 MHz signal generator, one 2.5 Gb/s LiNbO_3 modulator and one 10 Gb/s LiNbO_3 modulator on the output of TL_2 with injected power of 0.3 dBm and wavelength detune of +0.29 nm. The header of the two-level local signal is 10. The parameters of the local signal and the FP-LD are chosen such that the output control signal of the FP-LD at λ_c1 is at high level if the 1 in the local signal header coincides with the 1 in the data header, the
output at $\lambda_{c1}$ will be low otherwise. Thus the output control packet of the FP-LD is low for pk-1 and pk-2 but high for pk-3 and pk-4. A polarizer with perpendicular polarization state is used as an INV to select the TM mode. The inverted control packet is high for pk-1 and pk-2 but low for pk-3 and pk-4. For GEN-2, it is the same as GEN-1 but the header of the two-level local signal contains 01. Therefore, the output control packet of the FP-LD is low for pk-1 and pk-3 but high for pk-2 and pk-4. Consequently, the addresses of the output ports 1 to 4 of the 1×4 packet switch will be set to 00, 01, 10 and 11 respectively. Due to the symmetry in the design of proposed packet switch, we can use one SOA to observe the switched packets at different output ports. We observed that data packets with headers 00, 01, 10 and 11 transmit through Output 1, Output 2, Output 3 and Output 4 respectively. Independent bit error rate measurement has been carried out for each switched out data packet as shown in Fig. 4. The power penalty at BER of $10^{-9}$ is 2 dB.

4. Conclusions
We have successfully demonstrated all-optical packet routing in a 1×4 packet switch based on binary-encoded addressing scheme. The length of the address can be shortened from $N$ to $\log_2 N$ bits where $N$ is the total number output ports of all the nodes in the network. The power penalty at BER of $10^{-9}$ is 2 dB.

5. Acknowledgment
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6. Reference

Fig. 1. Schematic of the proposed all-optical memory. The all-optical memory is shown in dotted box.

Fig. 2. Experimental setup of the proposed switch.

Fig. 3. Synchronized timing diagrams correspond to the label in Fig. 1: (a) input data packets at the Input, (b) input local signal for GENs (the upper and lower inset show the header 10 for GEN-1 and 01 for GEN-2 respectively); (c) the control signal generated by GEN-1 (the inset is the corresponding inverted control signal); (d), (e), (f), and (g) are the switched data packets after passing through AOS-1, AOS-2, AOS-3 and AOS-4, respectively.

Fig. 4. Bit error rate measurements for each of the four switched out data packets.